IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13
7-6-04

Applicant:	Chambers	Docket No:	TI-30883
Serial No:	09/902,051	Examiner:	Davidson, Dan
Filed:	7/10/2001	Art Unit:	2651

For: CMOS DC OFFSET CORRECTION CIRCUIT WITH PROGRAMMABLE HIGH-PASS TRANSFER FUNCTION

APPEAL BRIEF PURSUANT TO 1.192(c)

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 6-22-04.

Tommie Chambers

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final Office Action mailed December 8, 2003 and the Advisory Action mailed March 17, 2004.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-10 were originally filed with no claims being cancelled. Thus, the subject matter of the instant appeal is the final rejection of Claims 1-10.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-10. No claims have been amended. A Response After Final, the Final Office Action was filed on March 8, 2004. The Advisory Action indicated that the Response had been considered, and consequently Appellants assume that it has been entered.

SUMMARY OF THE INVENTION

The present invention provides a high-pass filter that is switched on in response to thermal asperity. This high-pass filter has a high-pass pole which tracks the data rate by tuning a transconductance element of the high-pass filter so that it is proportional to the data rate clock. This results in the advantage of optimum DC offset suppression over a wide range of data rates corresponding to read back signals or the data signals distributed from the outer circumference of the magnetic disk (i.e., OD) to the inner circumference of the magnetic disk (i.e., ID). The present invention also includes a thermal asperity suppression mode that enables the high-pass filter to transition back to the normal mode in accordance with a gradual transition (as contrasted with a sharp transition). Thus, a gradual transition from a TA mode to an OFF mode minimizes amplitude and phase disturbances in the read back signal which can degrade BER and lead to the loss of timing recovery synchronization in the timing recovery loop. The gradual transition is accomplished by an attenuation block in that the gain of the attenuation block transitions from unity to zero in accordance, for example, with a slow exponentially decaying response.

The high-pass filter additionally includes an auto-zero mode so that the internal DC offset, which results from device mismatching, is canceled. This ensures that there is no shift in the corrected DC mode offset going from the normal mode to the TA suppression mode.

Figures 7 and 8 show a side and top view, respectively, of the disk drive system.

Figure 2 illustrates a block diagram of the invention.

A TA compensation high-pass filter circuit 202 is connected to a read channel analog front end 204. The read channel analog front end 204 is connected at its output to a A/D converter 206. Additionally, the output from the read channel analog front end 204 is connected to a TA detector 210. The output of the A/D converter 206 is connected to a read channel digital detector 208. Input to the TA detector 210 is a TA threshold signal to be compared with the output signal of the read channel analog front end 204. When the TA detector 210 detects a TA event, evidenced by the output signal from the read channel analog front end 204 which exceeds the TA threshold signal, an enable signal is output from the TA detector 210 and is input to the TA timer/control circuit 212. The TA timer/control circuit controls the TA compensation high-pass filter circuit by timing the duration of the activation of the TA correction high-pass filter 202. In accordance with the output signal from the TA timer/control circuit 212, the TA correction high-pass filter circuit 202 is turned appropriately ON or OFF.

Figure 3 illustrates a block diagram of the present invention.

Figure 4 illustrates more details of the circuit of Figure 3.

During normal operation, the high-pass filter is switched off so that the high-pass filter circuit 202 has a frequency response of unity refer to Figure 2. This is accomplished by setting $\alpha = 0$ in the ATTEN circuit 306 refer to Figure 3. When the TA event is detected, for example by the use of a slicer within TA detector 210 refer to

Figure 2, a timer is activated for the time period of the TA event. When the TA event is detected, the high-pass filter 202 is activated by switching the gain of the ATTEN block to one ($\alpha = 1$). This closes the feedback loop including transconductance circuit 308, the transconductance 304, and the attenuation circuit 306 which has a frequency response defined by equation 2 with a high pass pole given by Equation 1.

$$p = \frac{\alpha Gm_2 (Gm_3 \times RL)}{C}, A_V = Gm_1 RL \qquad (1)$$

$$H(s) = \frac{A_V (s/p)}{1 + (s/p)} \qquad (2)$$

The pole *p*, as illustrated above, determines how rapidly the DC offset is driven to zero.

The present invention is able to track the data rate by tuning transconductance 304 in Figure 2 so that it is proportional to the data rate clock. This is achieved by use of the tuning signal V_{TUNE}. This results in optimum DC offset suppression over a wide range of data rates corresponding to READ back signals distributed from the outer circumference of the magnetic disk (OD) to the inner circumference of the magnetic disk (ID).

Another feature of the present invention is that switching from the activation after a thermal asperity event back to normal operation is gradual. It is important that the high-pass filter pole frequency exhibit a gradual transition from the TA event to the OFF mode. This is done to minimize amplitude and phase disturbances in the read back signal, generated by the read channel, which can degrade BER due to loss of timing recovery synchronization (i.e., loss of lock). This gradual transition is accomplished by controlling the ATTEN circuit so that the gain (α) transitions from unity to zero with a slow

exponentially decaying response. Other responses are possible. Additionally, the high-pass filter 202 in Figure 2 is engaged during the auto-zero mode so that the internal DC offset, which is the result of device mismatching, at the output of the high-frequency filter 202 output is reduced.

The waveform input to the ATTEN circuit is illustrated in Figure 5. Figure 5a illustrates the voltage V_{ATTEN}, applied to the ATTEN circuit 306, for auto-zero mode, and Figure 5b illustrates the voltage V_{ATTEN}, applied to the ATTEN circuit 306, for a thermal asperity event.

ISSUES

The sole issue on appeal is whether or not Claims 1-10 are anticipated under 35 U.S.C. § 102(e) as being anticipated by Patti.

GROUPING OF THE CLAIMS

Each of Claims 1 and 6 as contained in the attached Appendix, is independently patentable, and these rejected claims do not stand or fall together for the reasons more clearly set forth herein below.

ARGUMENTS

It is respectfully submitted that Patti does not disclose or suggest the presently claimed invention including a filter circuit to respond to the thermal asperity signal in accordance with the data rate.

The Examiner alleges that Patti discloses an offset correction circuit to correct DC offset in accordance with a data rate referring to Figure 3 element 102, Figure 2a, and column 6, lines 51-56.

Notwithstanding the allegations of the Examiner, Patti discloses at column 6, lines 51-56 that the programmed resistances of the variable resistance circuit 132 are selected to achieve the cutoff frequencies for the filter 112. The programmable thermal asperity recovery circuit 132 provides flexibility allowing utilization in read channels having potentially different or varying characteristics (citing different data rates, different causes for the thermal interference, etc.).

The resistance circuit 132 does not respond to data rates.

Patti does not disclose a circuit to determine the data rate and consequently there is no way of adjusting the programmable thermal asperity recovery circuit based on different data rates.

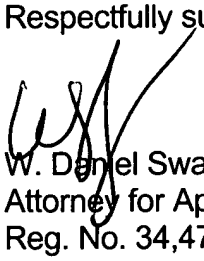
Claims 1-10 patentably define over the applied art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 under 35 U.S.C. § 102 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

APPENDIX

1. An offset correction circuit to correct DC offset in accordance with a data rate, comprising:

a detection circuit to detect a thermal asperity signal; and

a filter circuit to respond to said thermal asperity signal in accordance with said data rate.

2. An offset correction circuit, as in Claim 1, wherein said filter circuit affects said DC offset in accordance with said data rate.

3. An offset correction circuit, as in Claim 1, wherein said filter circuit is a transconductance circuit.

4. An offset correction circuit, as in Claim 3, wherein said transconductance circuit shunts current in accordance with said data rate.

5. An offset correction circuit, as in Claim 3, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.

6. A disk drive system for reading and writing information on a disk, comprising:

a head to read/write information on said disk;

a preamplifier to amplify said information; and

a read channel to process said amplified information, said read channel including:

an offset correct circuit to correct DC offset in accordance with a data rate, said offset correction circuit including:

a detection circuit to detect a thermal asperity signal; and

a filter circuit to respond to said thermal asperity signal in accordance with said data rate.

7. A disk drive system, as in Claim 6, wherein said filter circuit affects said DC offset in accordance with said data rate.

8. A disk drive system, as in Claim 6, wherein said filter circuit is a transconductance circuit.

9. A disk drive system, as in Claim 8, wherein aid transconductance circuit shunts current in accordance with said data rate.

10. A disk drive system, as in Claim 8, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.